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(71) Applicant(s)
Simage OY
(Incorporated in Finland)
Teknikantie 12, 02150 Espoo, Finland

(72) Inventor(s)
Jouni Ilari Pyyhtia
Markku Tapio Eraluoto

(74) Agent and/or Address for Service
D Young & Co
21 New Fetter Lane, LONDON, EC4A 1DA,
United Kingdom

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(54) Abstract Title
Controllable resolution imaging array

(57) An imaging device for radiation imaging consists of an array (80, 82, 84) of detector cells and an array of image cell circuits. Each detector cell is connected to the corresponding cell in the array of image cell circuits. Each individual cell in the detector cell array generates a charge based on the radiation that hits the cell. Each cell in the array of image cell circuits accumulates the charge in a storage capacitor. The storage capacitor can be, for example, the gate of a transistor. Single detector cells (86) can be grouped together to form larger area super cells (88, 90), the size of which can be controlled by control signals, which select the operating mode. The output from a single cell or a super cell is read out in current mode and the output from a super cell is scaled according the size of the cell to produce an average current. Several modes can be implemented in the imaging device. Also, an imaging system for larger area radiation imaging can be implemented by connecting several imaging devices together in the form of a two dimensional array.

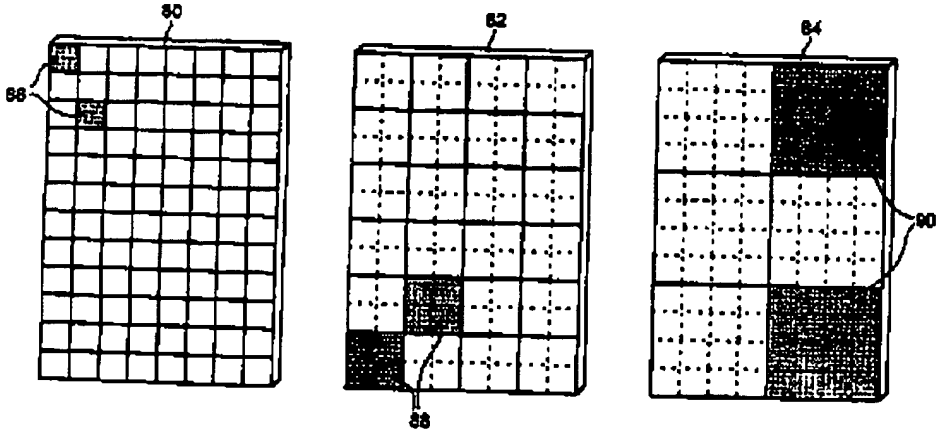

FIG. 4

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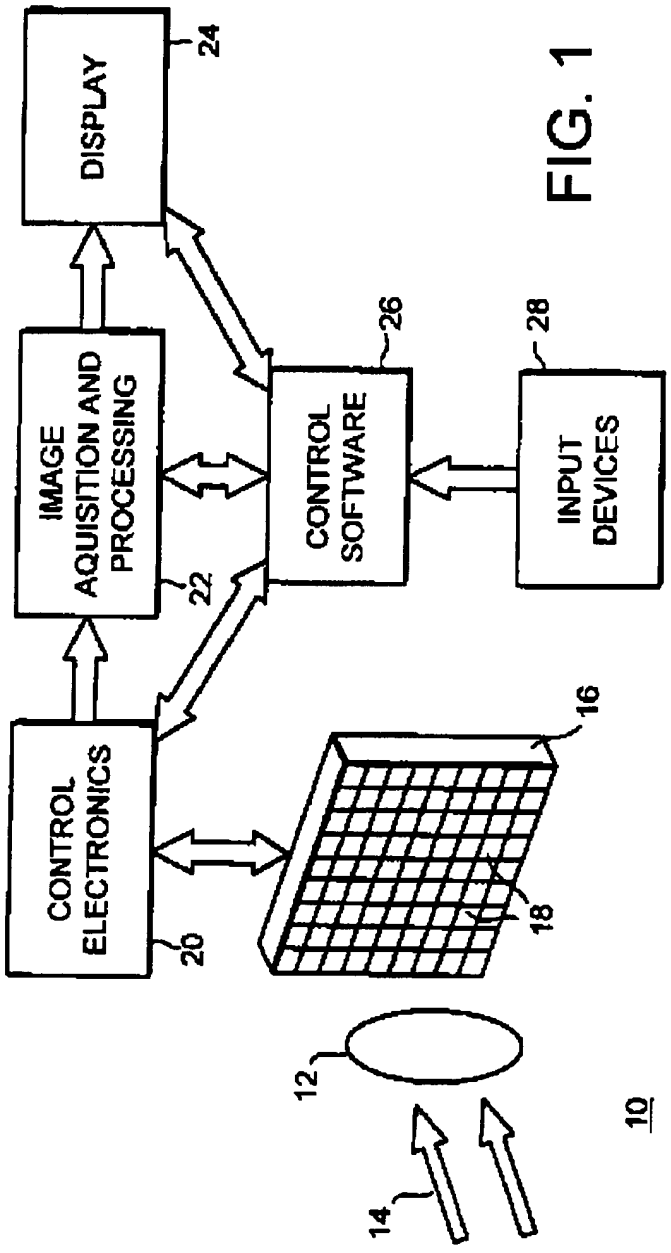

DISPLAY
24
IMAGE AQUISITION AND PROCESSING
22
CONTROL SOFTWARE
26
INPUT DEVICES
28
CONTROL ELECTRONICS
20
16
18
12
14
10

FIG. 1

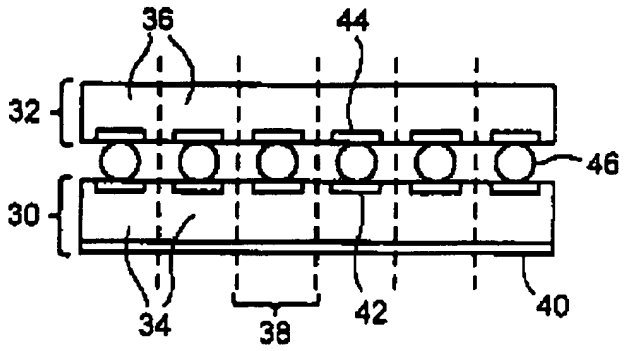

36
44
32
46
30
34
38
42
40

FIG. 2

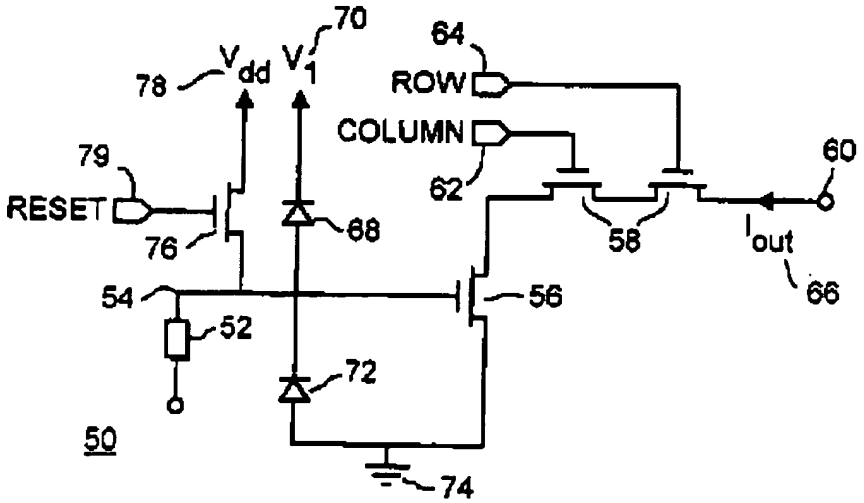

70
64
78
V_{dd}
V_1
ROW
COLUMN
79
60
62
RESET
68
58
I_{out}
76
54
56
66
52
72
50
74

FIG. 3

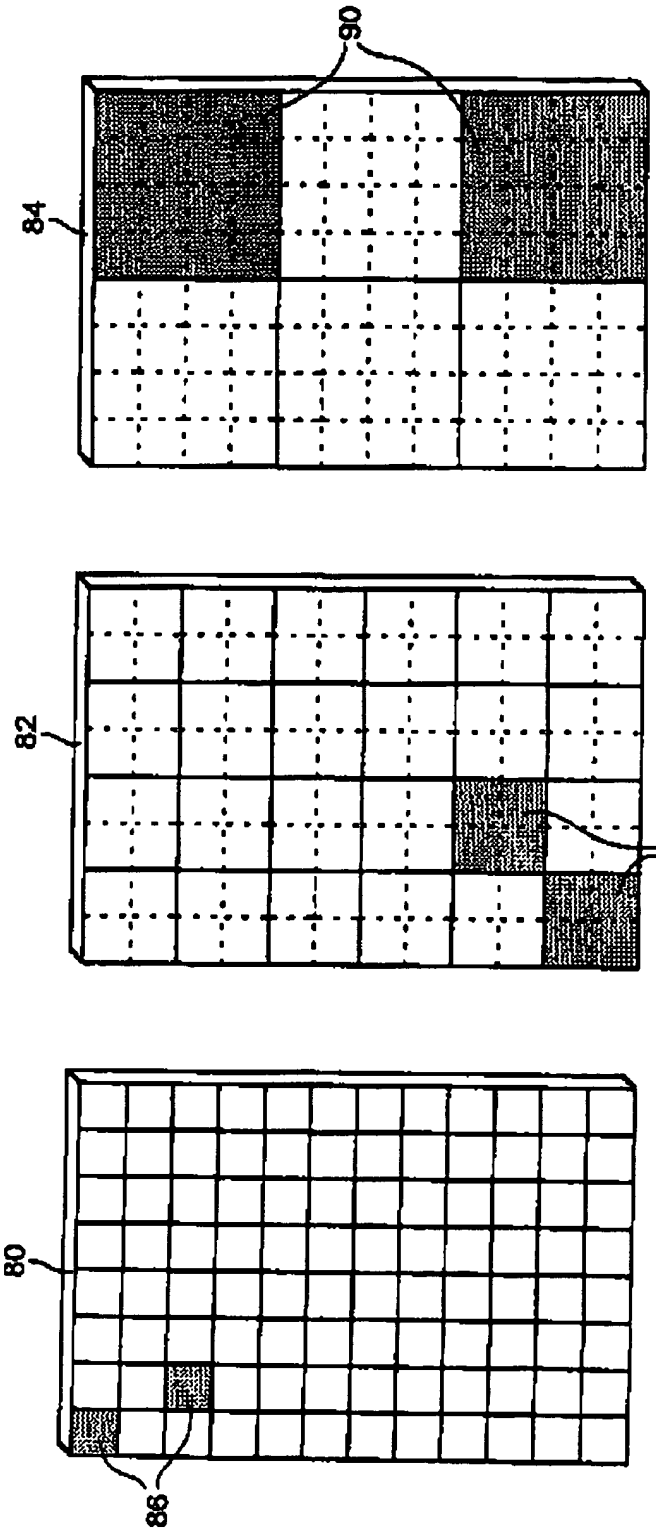
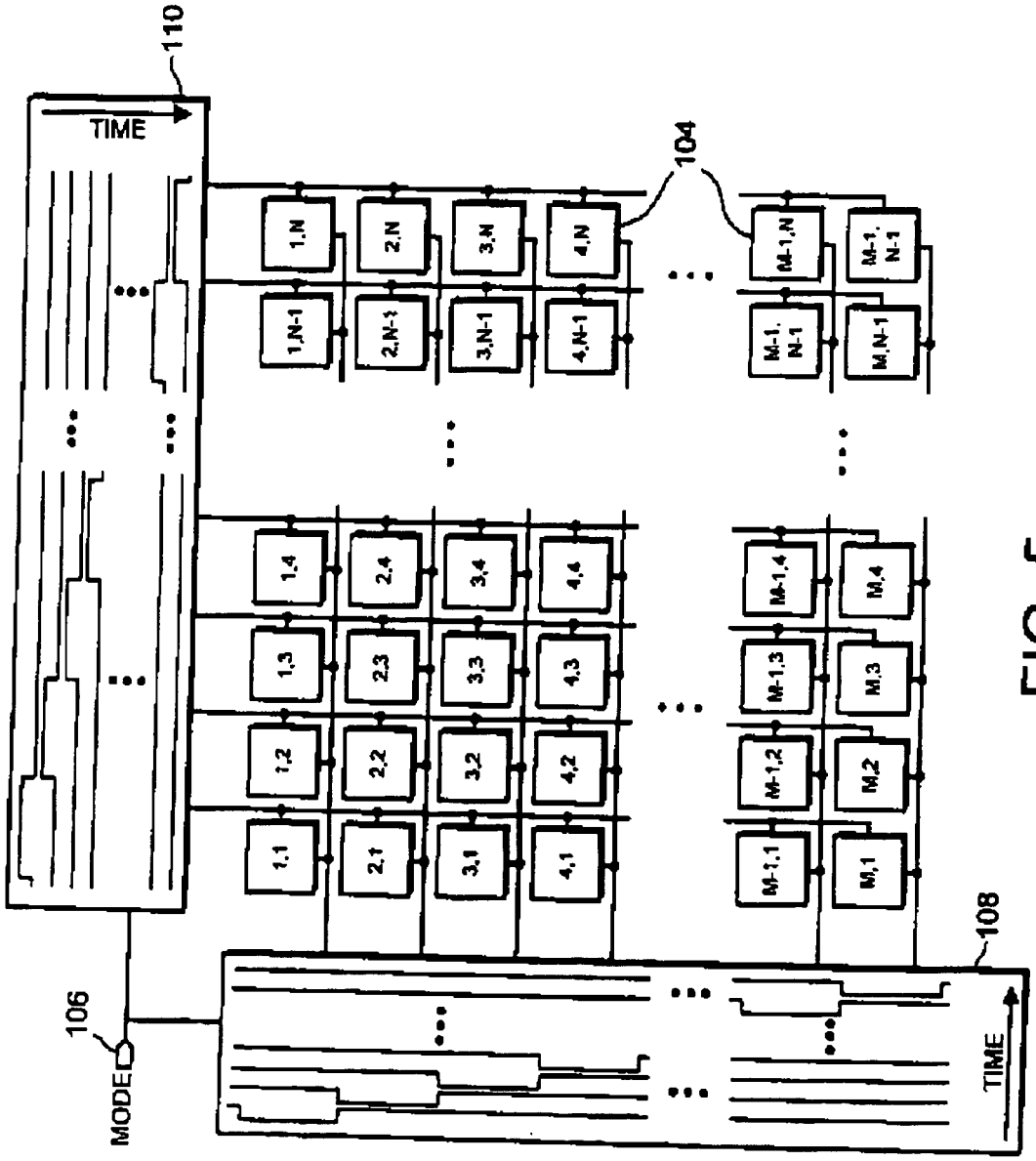


FIG. 4


110
TIME
104
1,N
2,N
3,N
4,N
M-1,N
M,N
1,N-1
2,N-1
3,N-1
4,N-1
M-1,N-1
M,N-1
1,4
2,4
3,4
4,4
M-1,4
M,4
1,3
2,3
3,3
4,3
M-1,3
M,3
1,2
2,2
3,2
4,2
M-1,2
M,2
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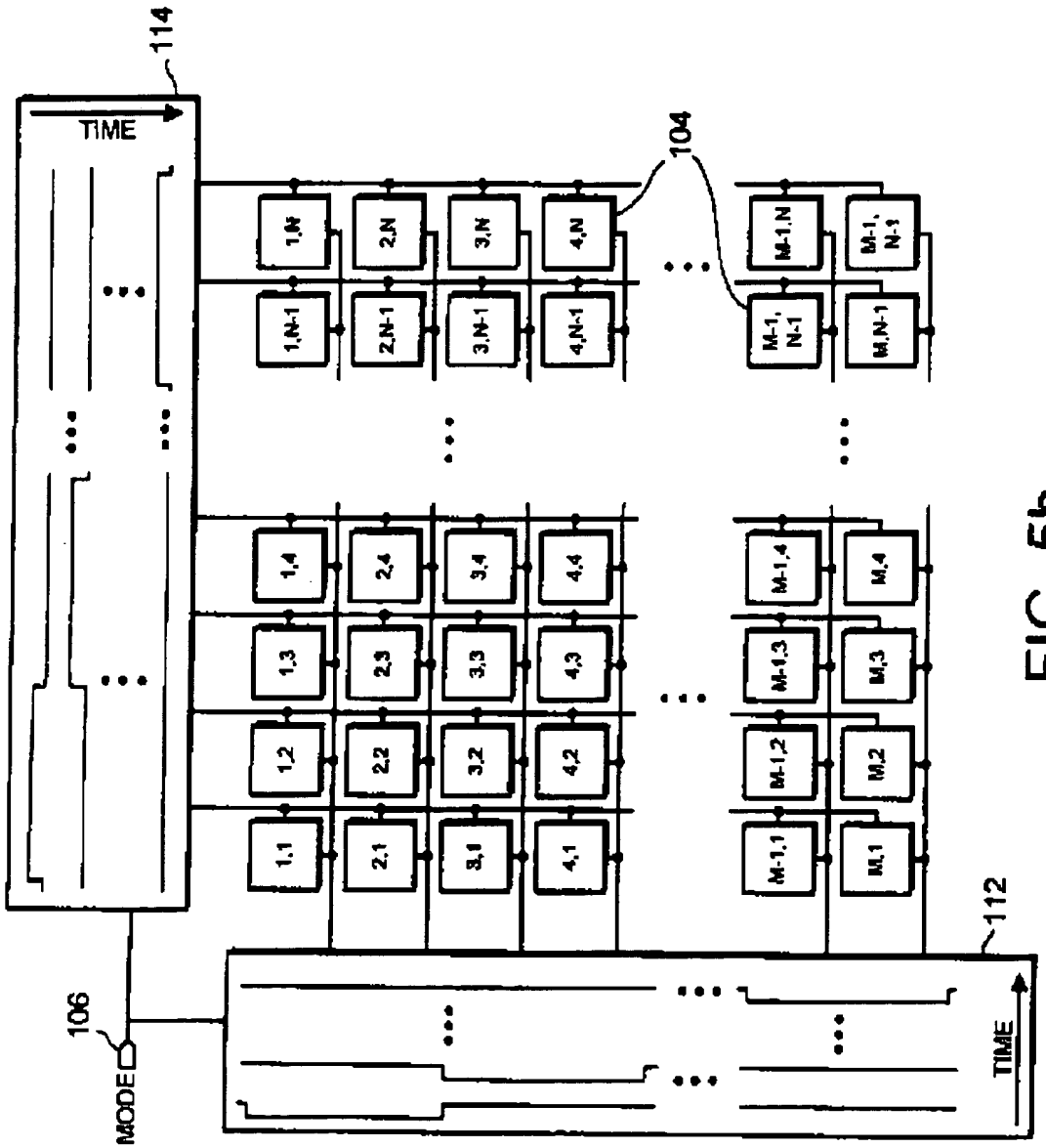
3,1
4,1
M-1,1
M,1
108
106
MODE
TIME
100

FIG. 5a


114
TIME
104
1,N
2,N
3,N
4,N
M-1,N
M,N
1,N-1
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4,N-1
M-1, N-1
M,N-1
1,4
2,4
3,4
4,4
M-1,4
M,4
1,3
2,3
3,3
4,3
M-1,3
M,3
1,2
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3,2
4,2
M-1,2
M,2
1,1
2,1
3,1
4,1
M-1,1
M,1
112
102
106
MODE
TIME

FIG. 5b

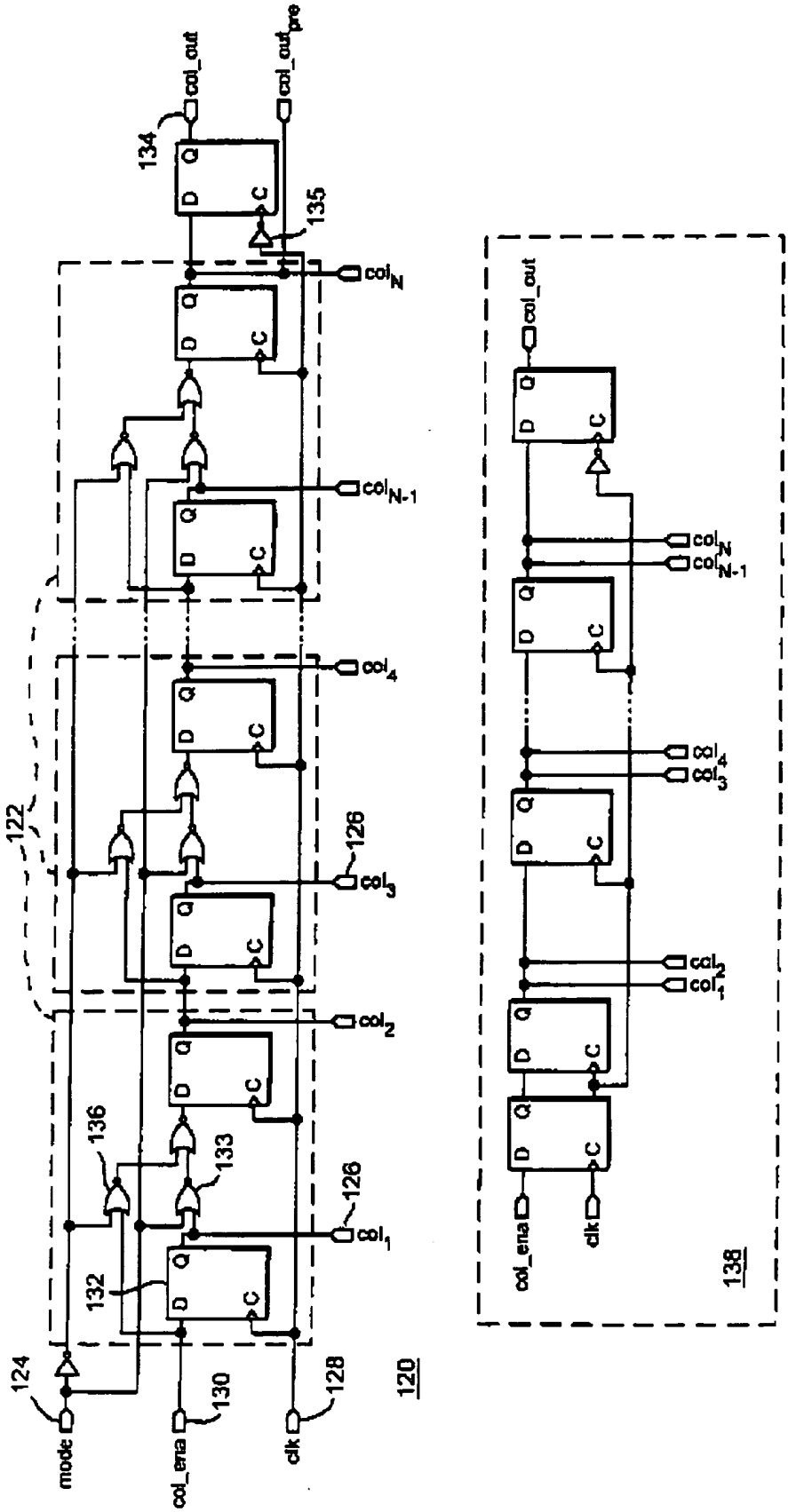
col_out
col_out_pre
134
135
col_N
col_N-1
col_4
col_3
col_2
col_1
126
122
136
133
132
124
130
128
mode
col_ena
clk
120
col_out
col_N
col_N-1
col_4
col_3
col_2
col_1
col_ena
clk
138

FIG. 6

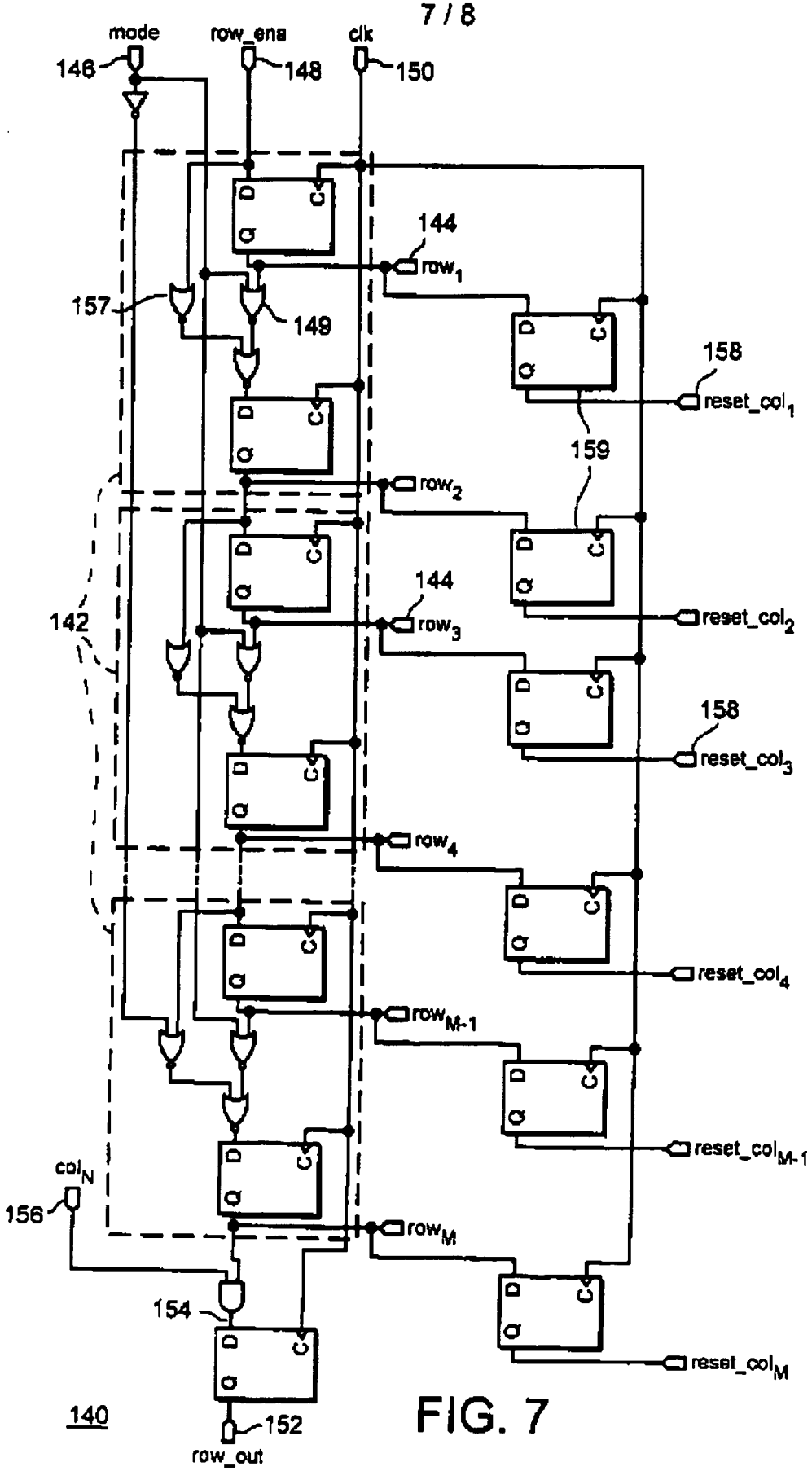
mode
row_ena
clk
146
148
150
144
row1
157
149
158
reset_col1
159
row2
144
row3
142
reset_col2
158
reset_col3
row4
reset_col4
rowM-1
reset_colM-1
colN
156
rowM
154
reset_colM
140
152
row_out

FIG. 7

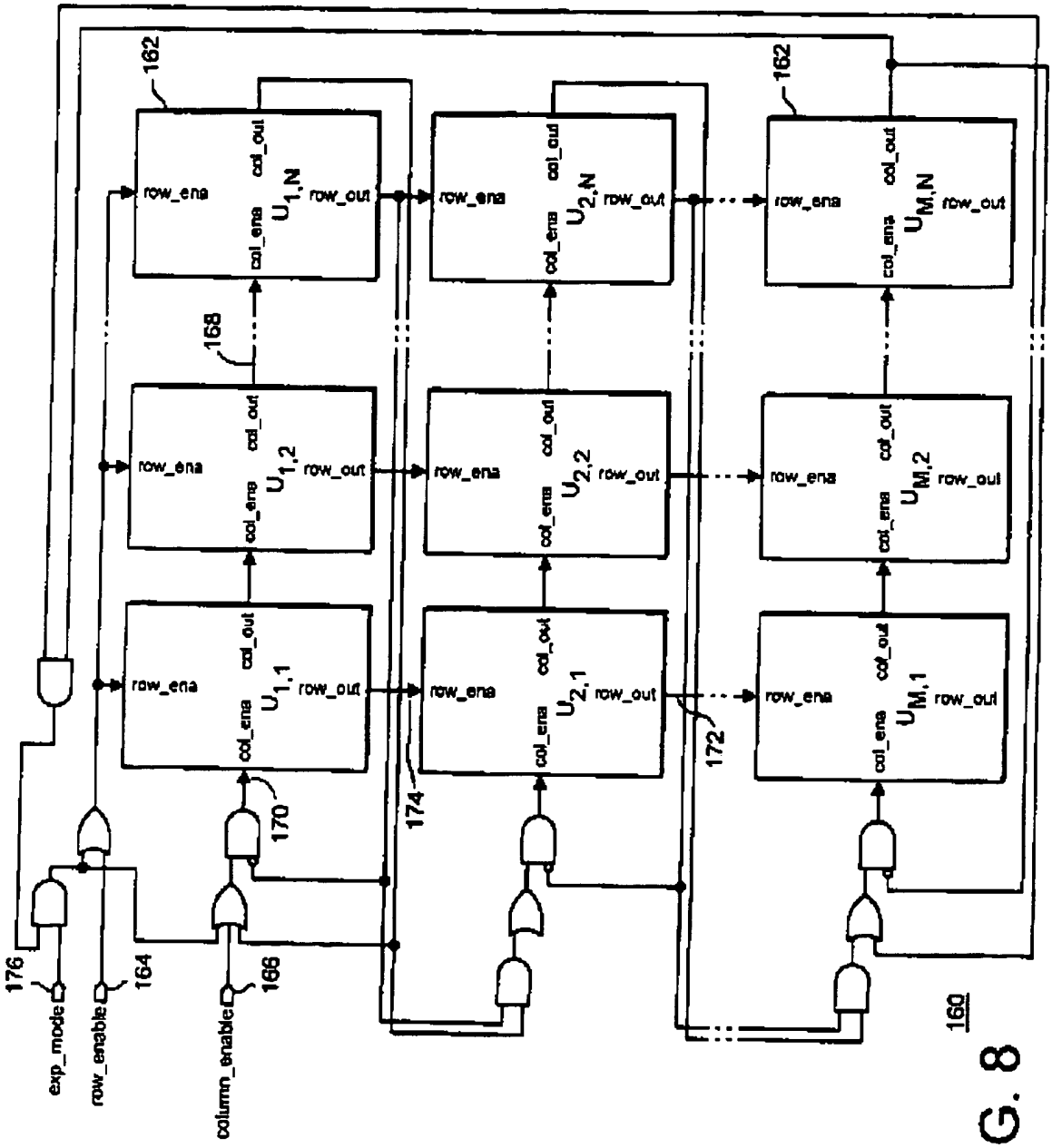
162
168
row_ena
col_out
col_ena
row_out
$U_{1,N}$
$U_{2,N}$
$U_{M,N}$
$U_{1,2}$
$U_{2,2}$
$U_{M,2}$
$U_{1,1}$
$U_{2,1}$
$U_{M,1}$
170
172
174
176
164
166
exp_mode
row_enable
column_enable
160

FIG. 8

DEVICE FOR IMAGING RADIATION

This invention relates to radiation imaging using a semiconductor imaging device consisting of an array of image cells.

This invention describes a semiconductor imaging device for radiation imaging. The imaging device is an array of image cells, which consists of an array of radiation detector cells and an array of image cell circuits. An example of an imaging system configuration is shown in Figure 1 of the accompanying drawings. All cells in the detector cell array are connected to respective electronics cells in the array of image cell circuits. With appropriate processing technology, it is possible to implement both detector cells and circuit cells on the same substrate. Another possibility is to have two substrates, one for the detector and one for the cell circuits and, by using a bump-bonding or other technique connect them mechanically and electrically together so that each detector cell is connected to the corresponding cell circuit. A cross-section of a part of an imaging device made of two substrates, which are bump-bonded together, is shown in Figure 2 of the accompanying drawings.

In many radiation imaging applications, a need for different image resolutions exist. In single exposure images, the resolution should usually be relatively high. On the other hand, the same imaging system could be used for displaying live image by continuously reading the image from the imaging device and updating the display in real time. However, if the imaging system is designed for high resolution, the data bandwidth for a live image at, for example, 30 frames per second may be so high that the requirements for the readout electronics for handling the data stream may become unreasonable. A readout system fast enough to capture and process the images could become unreasonably expensive compared to the total cost of the imaging system. Furthermore, a high image resolution required for single exposure images may not even be required for a live display of images.

Therefore, a method for effectively reducing the resolution and thus the data bandwidth on chip would solve the problem. Another problem is the scalability of the imaging system for large or small area imaging systems. If single imaging devices with relatively small area could be easily linked together to form a seamlessly

connected array of imaging devices for large area imaging system, the same imaging devices could easily be used for either large and small area applications.

This invention tries to solve the problems addressed above by introducing an imaging device with programmable image resolution and simple tiling of the devices to make a flexible imaging system for wide variety of target applications.

Particular and preferred aspects of the invention are set out in the accompanying independent and dependent claims. Features from dependent claims may be combined with those of the independent claims in any appropriate manner and not merely in the specific combinations enumerated in the claims.

In accordance with one aspect of the invention, there is provided an imaging device for radiation imaging, the device comprising an array of detector cells for generating a charge in response to incident radiation, an array of cell circuits for accumulating charge generated, and control circuitry controlling output of signals from the cell circuits programmably to adjust the resolution of the imaging device.

The array of detector cells and the array of cell circuits form an array of pixels. As a result of the programmable resolution, an imaging device according to the invention can provide different operational modes giving different pixel resolutions for different target applications.

In a preferred embodiment, the programmability in that the control circuitry is arranged to select a group of cell circuits and to produce an output signal representative of a sum of charge accumulated in all cell circuits in a group. Thus, the control circuitry enables grouping of several pixels together to form a larger area super pixel for lower resolution imaging.

In a preferred embodiment the control circuitry averages signals representative of charge accumulated in all cell circuits in a group. For example, the output signal is representative of the total charge for all of the cell circuits of a group divided by the number of cell circuits in the group. Preferably, the number of cell circuits in a group is selectable from a set of possible numbers.

In a preferred embodiment, the output signal representative of charge accumulated is a current value. The use of a current output facilitates circuitry required to combine and average signal levels.

The control circuitry, for selecting a group of cell circuits, comprises a shift register arranged to select a plurality of columns or rows concurrently and to advance in steps of more than one row or column. The control circuitry can additionally comprise logic arranged simultaneous to select a plurality of rows and columns and a step size larger than one.

The control circuitry is arranged to average currents from a group of cell circuits by connecting current outputs of each cell circuit into a common output node and dividing the resulting sum of currents by the number of pixels in the group using a current mirror. The common output node can hold a current of the selected cell circuit(s).

Alternatively, for implementing group modes, each cell circuits in a group can be arranged to produce a scaled output signal representative of charge accumulated in the cell circuit divided by a number of cell circuits in the group. In order to be operable in a plurality of group modes, where each group mode has associated with it a predetermined number of cell circuits, the cell circuits can be arranged to include an output transistor for each group mode, which output transistor produces a scaled output signal according to the number of cells in a selected group mode. The output signal from all cell circuits in the group can then be averaged by summing the signals together.

In an embodiment of the invention, the resolution is controlled from outside by one or more control signals. For example, with two control signals, four different modes for resolution can be achieved. Thus, separate enabling signals can be provided for selecting columns and rows and output signals for indicating end of row or end of column.

In an embodiment, end of row and end of column output signals of one device are connected to corresponding enabling signals of an adjacent device in first and second orthogonal directions, respectively, to form an array of imaging devices for larger area radiation imaging.

Thus, in an embodiment of the invention, in addition to a mode where every individual pixel is read, 2x2, 3x3 or 4x4 pixels could be grouped together and read out as super pixels. Other pixel combinations (for example having different numbers of

rows and columns) and different number of modes can be used as well. The summation of pixel values can be easily done since the summation is done in current mode. Output currents of several cells are connected together. Adding currents from several cells together results in larger overall current. This can be compensated by an additional current mirror, which scales the current output to the same range as the current output of a single cell. In other words, the current mirror divides the current from a super pixel by the number of cells in the super pixel. This is equivalent to taking an average of a larger number of individual pixels. Using current mode output also has another advantage, enabling longer wiring without losing accuracy. Performing the averaging of pixel values is by no means limited to using current output. Voltage mode can be used instead of the current mode as described hereinafter. Using voltage mode would require the voltages of several pixels to be summed and averaged by using, for example, an op-amp circuit.

Moreover, an embodiment of the invention thus provides a solution to the problem of providing a video scan output from a imaging device constructed from a plurality of readout devices. Thus rather than reading out a device at a time, a large area imaging system formed from small area readout devices can be read one line from the whole imaging area before advancing to the next row of pixels. Together the readout devices form a seamless large area imaging system enabling scanned output over the whole image area. The imaging device has two input signals, which start the sequence for selecting the column and row for output. Furthermore, the imaging device has two outputs, one of which indicate when the last pixel of each line has been read and the other indicates when the last row of the device has been read. These output signals are connected to the corresponding input signals in the adjacent imaging devices in horizontal and vertical direction. The column and row output from the last imaging device can be connected to the first device to make the system run in a continuous mode for live video applications. The mode is selectable so that the user can switch between the single exposure mode and the live video mode at any time.

The combination of the above mentioned features makes it possible to use the same system for making single exposures with high resolution and at any time

switching to live video mode and at the same time changing to lower resolution to reduce the data bandwidth. The size of the pixels is not fixed to any physical dimensions, but can be scaled according to available processing technology and based on the requirements of the target application.

The invention also provides an imaging system, comprising a plurality of imaging devices according to as defined above connected as a two-dimensional array, whereby the imaging system provides selectable imaging resolutions for selected applications. Control circuitry can permit reading of cell circuits one row at a time from the two-dimensional array of imaging devices, as opposed to one imaging device at a time.

In accordance with another aspect of the invention, there is provided a method of operating an imaging device for radiation imaging, which device comprises of an array of detector cells for generating a charge in response to incident radiation, an array of cell circuits for accumulating charge generated, and control circuitry controlling output of signals from the cell circuits, the method comprising:

selecting a resolution of the imaging device;

adjusting addressing of the cell circuits to group outputs from the cell circuits according to a selected resolution.

Exemplary embodiments are described by way of example only with reference to the accompanying drawings, in which:

Figure 1 shows an overall imaging system for radiation imaging.

Figure 2 depicts an example of a cross-section of an imaging device comprising of a pixel array.

Figure 3 shows a schematic diagram of one cell of image electronics.

Figure 4 illustrates the grouping of pixels into larger area super pixels.

Figure 5 shows a two-dimensional pixel array with control signals for selecting output pixels.

Figure 6 shows an example of a schematic diagram used for selecting columns in a pixel array.

Figure 7 shows an example of a schematic diagram used for selecting rows and resetting rows of pixels in a pixel array.

Figure 8 illustrates imaging system consisting of an array of imaging devices and with two modes of operation: single shot and continuous.

Figure 1 shows an example of an imaging system for radiation imaging including an imaging device according to the invention. The imaging device is intended for imaging of high-energy radiation, for example X-ray radiation. However, the invention is not limited to imaging of high-energy X-ray radiation, but can be applied to detection of any type of radiation, for example α-ray, β-ray, γ-ray, infra red or optical radiation, subject to choice of appropriate semiconductor substrate for the detector.

The imaging system 10 in Figure 1 provides imaging of an object 12 subject to radiation 14. The object may, for example, be part of a human body in case of medical imaging or any other object, in case of non-destructive testing.

The imaging device 16 in Figure 1 can consist of one or two semiconductor substrates. In case of one substrate, each cell 18 in the substrate comprises of a pixel detector and a pixel circuit. Alternatively, two substrates can be used, one containing an array of detector cells while an array of pixel circuits is located on another substrate. The two substrates can, for example, be connected using a bump-bonding or other technique, as described below.

Each detector cell on the imaging device 16 detects high-energy radiation and generates a charge, which is accumulated on a capacitor in the corresponding image cell circuit. After a certain iteration time, the charge is read out from the cell circuits as a current representative of stored charge, one cell at a time. The control electronics 20 create the necessary signals for starting the iteration and resetting the cells to a predefined value after the iterated charge has been read. The current from each cell is amplified and scaled before converting it to a digital signal, or word in the image acquisition unit 22. The digital information is further processed in the image processing unit 22 to create a desired result. For example, calibration of individual pixels can be done in the image processing unit 22 in order to compensate for the non-uniform response of pixels in the array. Process variations in fabrication of the detector array or the electronics array may lead to pixels having a non-uniform response to a uniform level of radiation. This can be compensated by post-processing

of the image before displaying it on the display 24. The control electronics 20, image acquisition and processing unit 22 and the image display unit 24 can all be located inside a computer running application software 26, which controls the whole system according to user inputs via input devices 28, such as keyboard or mouse.

Figure 2 is a cross-section of part of an imaging device. The imaging device consists of a detector substrate 30 and a readout substrate 32. In Figure 2, the two substrates are connected together by a bump-bonding technique. The detector and readout substrates consist of an array of detector cells 34 and an array of cell circuits 36, respectively. The detector cell and the cell circuit form an image cell 38. The detection area of a detector cell 34 for the imaging cell 38 is defined between a continuous electrode 40 and by a pixel electrode 42. The continuous electrode on the detector substrate is used for applying a bias voltage. On the image electronics substrate, the contacts 44 for the pixel cells are at the corresponding locations to the electrodes on the detector substrate. A detector cell and the corresponding cell circuit are connected by means of a bump-bond 46.

The physical size of the image cell 38, consisting of a pixel detector cell 34 and corresponding circuit cell 36, is not fixed but can be designed according to the requirements of the target application and within the limits of available processing technology for integrated circuit manufacturing. Also, with an appropriate semiconductor process, detector cells 34 and the corresponding cell circuits 36 can be implemented on a same substrate. Thus, with suitable technology, the invention is applicable to single substrate implementation as well as the dual substrate technique described herein.

The material for the detector substrate 30 and readout substrate 32 can be chosen according to the application and availability of suitable processing technologies. For example, silicon can be used for both substrates. Other materials can be used as well. For example, the detector substrate could be fabricated of CdZnTe, CdTe, HgI2, InSb, GaAs, Ge, TlBr, Si and PbI.

Figure 3 depicts a schematic diagram of the image cell circuit 50. Each pixel or image cell in the array comprises a similar cell circuit. In Figure 3, the detector cell is represented by 52. The input of the cell circuit, node 54 corresponds to the

bump-bonded connection between the detector cell and the cell circuit. When radiation ionizes the detection zone in the detector, an electronic charge is created and accumulated on the gate capacitance of the memory transistor 56. Two transistors 58 are used as switches between the drain of the memory transistor 56 and the output node of the cell 60. When the column 62 and row indicator signals 64 for the cell are active concurrently, the drain of the transistor 56 is connected to the output node 60 of the cell and the drain current 66 of the memory transistor can be read out. The drain current is a function of the gate-source voltage of the transistor and thus represents the charge accumulated on the gate capacitance of the transistor 56.

Overflow of the gate voltage is protected by a diode 68 connected between the gate of the memory transistor 56 and V_t 70. Similarly, underflow is protected with a diode 72 between ground (GND) 74 and the gate of the transistor 56. An additional transistor 76 is used for resetting the gate voltage of the memory transistor 56 to a predefined reset voltage value V_{reset} 78 every time the reset signal 79 is active.

The grouping of pixels into larger area super pixels is represented in Figure 4. Three imaging devices 80, 82 and 84 are shown in the Figure 4. The imaging device 80 illustrates a device with no pixel grouping. The image is read one pixel 86 at a time. Using control signals for selecting the mode of operation, the pixels in imaging devices can be grouped in to larger clusters. Figure 4 illustrates three different modes of operation, imaging device 80 with no grouping, imaging device 82 with grouping of 2(2 pixels into one super pixel 88 and imaging device 84 with grouping of 4(4 pixels into one super pixel 90. The number of modes used in an actual application is by no means limited to the ones shown in this example but can be freely chosen according to the requirements of a particular application.

With further reference to Figure 3, if the imaging device is used in a group mode, the output currents from all the cells in the group can be summed together and divided by the number of cells in the group in order to produce an averaged output. An alternative way of implementing the same averaging is to make the division on the cell itself before summing the current outputs together. In order to do this, several memory transistors 56 having different characterisitics can be implemented in each cell circuit. Thus, each cell can produce several outputs with different scaling values

dependent on different group sizes. In each group mode, a different output is selected by a selection signal (not shown) according to the size of the group. The output currents from the cell circuits, which are already divided by the number of pixels in the group, is then summed to produce an averaged output.

Figure 5 illustrates two identical imaging devices consisting of a two-dimensional pixel array. Also, control signals for selecting the output pixel(s) are shown in Figure 5. The array is of size *MxN*, where *M* is the number of pixels in vertical direction and *N* is the number of pixels in horizontal direction. Imaging device 100 in Figure 5a uses operating mode in which every pixel is read, i.e. no grouping of pixels is used. The imaging device 102 in Figure 5b is operating in a mode, which groups 2x2 pixels into one super pixel. Pixels 104 in Figure 5 are indicated as Y,X, where X and Y represent the horizontal and vertical location of the pixel in the two-dimensional pixel array, respectively. The imaging device has control logic which generates the required signals for selecting the right column and row in the pixel array, according to the selected mode. The mode is selected with the mode signal 106. In Figure 5a, the control logic 108 generates the signal, which selects one row at a time, starting from the first row. While the first row is selected, the control logic 110 generates a signal, which selects the first column. On each clock cycle, the column selector 110 advances to the next column until last column of a row is reached. When the last column of the first row is finished reading, the row selector 108 is advanced to the next row. This is repeated until last row is read. The resetting of the pixels can be done one row at a time, so that the reset signal generated for the row is the row-selecting signal delayed by one clock cycle.

The imaging device 102 in Figure 5b operates in a different mode compared to the device 100 in Figure 5b. In this mode two columns and two rows are selected simultaneously. The operation of the row selector 112 is identical to the operation of row selector 108 in Figure 5a except for the operating mode, where two rows are selected simultaneously and the selector is advanced in two row steps. Similarly, the column selector 114 operates in the same way as the column selector 110 except for selecting two columns at a time and advancing in two column steps. The control logic for row and column selectors can be designed to include as many operating modes for

grouping pixels as necessary for the target application. In this example only two modes with no grouping and grouping of 2x2 pixels were shown, but the number of built-in modes is not limited in any way. Inside the control logic boxes 108, 110, 112 and 114 in Figure 5, the control signals are shown at various instants in time, indicating the selection of pixels. When both the column and row selector for a pixel is selected, its output current can be read in the output node of the device.

Figure 6 illustrates an example schematic diagram for the control logic 120 that is used for selecting columns of a pixel array. A pixel is selected by selecting a row and a column simultaneously. The control logic 120 in Figure 6 consists of building blocks 122, each of which contain the necessary logic for selecting one or two columns in a two column group. The building blocks form a shift register with the required logic to enable grouping of pixels. Counters or other logic, which perform the same function can be used for selecting rows or columns as well. Two modes of operation are included in the logic in Figure 6. The two modes are: no grouping and groups of two columns. The mode is controlled by a control signal 124. When the mode signal 124 is in logic low level, the logic operates in normal mode, selecting one column 126 at a time and advancing to the next column at each clock cycle 128. The sequence is started by the *col_ena* signal 130. At the first clock cycle the state of the *col_ena* signal 130 is stored in the flip-flop 132, selecting first column. In this mode, the signal propagates through the gate 133 and the output of the first flip-flop is connected to the input of the second flip-flop. In each building block in the control logic 120, the signals are connected identically. One column is selected at a time and at each clock cycle the signal propagates to the next flip-flop selecting the next column in the chain. When the last column is selected, the control logic 120 produces an output signal *col_out* 134 so that one device can be connected to another to form a continuous array as explained later. The inverter 135 is added to invert the clock signal 128 in order to produce the *col-out* output signal at the correct time so that the sequence of selecting columns is continued in the next imaging device without delay.

If the mode signal 124 is in logic high state, the control logic 120 operates in a grouping mode where two columns are selected simultaneously and advanced two columns at a time at each clock cycle 128. In this mode the signal propagates through

the gate 136 instead of gate 133, so that the input of the first flip-flop 132 is also the input for the next flip-flop. This enables the flip-flops to change state simultaneously, selecting two columns at a time. In this mode the operation of the control logic 120 is identical to the operation of the control logic 138, where the selection signals of two successive rows are connected together. When similar logic is used for selecting rows, this mode selects groups of 2x2 pixels. In this example only two modes of operation are available, but the number of modes is by no means limited to these modes. Any number and combination of different modes can be included in the row and column selecting logic using the same principle as shown in Figure 6. The number of mode inputs depends on the number of modes included in the design.

Figure 7 illustrates an example schematic diagram for the control logic 140 that is used for selecting rows from an array of pixels. As mentioned above a pixel is selected for output when both a column and a row corresponding to the location of the pixel are selected simultaneously. The row selecting logic is similar to the one used for selecting columns but additional logic is used for resetting rows of pixels. The control logic 140 consists of building blocks 142. Each building block contains the necessary logic for selecting one or two rows 144 at a time depending on the state of the *mode* input 146. The row selecting sequence of the control logic 140 is started by a pulse in *row_ena* input signal 148. If the *mode* signal is in the logic low state, one row is selected at a time. In this mode the signal propagates through the gate 149 so that the output of each flip flop is connected to the input of the next flip flop. At each clock cycle the signal propagates from one flip flop to the next, selecting one column at a time. At each clock cycle 150 the next row is selected until the last row is reached. The *row_out* signal 152 is generated when both the last row (row_M) and the last column (col_N) are both selected. Therefore, the input to the D-flip flop producing the *row_out* signal 152 is generated from the selection signal of the last row (row_M) and the selection signal for the last column (col_N) 156 by a logical AND gate.

If the *mode* signal 148 is in the logic high state, the control logic selects two rows at a time and advances in steps of two at each clock cycle 150. In this mode the selection signal propagates through the gate 157 instead of gate 149, grouping the inputs of the two flip flops in each building block together so that they change state

at the same time, i.e. two rows are selected at a time. At each clock cycle, the selection is advanced at two row steps. Using same mode for rows and columns, 2x2 pixels are grouped into one super pixels when the mode signal is in the logical low state. Any number or combination of modes for selecting rows and columns can be used instead or in addition to the two modes used in 140.

The reset signals 158, which are used for resetting a row of pixels to a predefined value, are produced from the corresponding row selection signals 144 by delaying them one clock cycle using D-flip flops 159. The operating mode for grouping pixels does not effect the operation of reset logic in any way. If grouping is used, several rows of pixels are reset simultaneously.

Figure 8 shows an example of an imaging system 160 consisting of an array of imaging devices. The array consists of MxN imaging devices, connected together to form a continuous imaging area. Each imaging device 162 in the array of imaging devices includes the logic for programmable resolution described above. This example illustrates the connections between devices 162 using the enable and out signals for rows and columns, which are available in each imaging device. The imaging system is started using the *row_enable* 164 and *column_enable* 166 signals. Once started, the first row and the first column of the first imaging device, marked $U_{1,1}$, is selected for output. The column selector advances at each clock cycle and when the last column of the first row is read, a *col_out* signal 168 is produced. The *col_out* signal 168 is connected to the *col_ena* input 170 of the next device in the array. The reading of pixels is continued from the first row of the next device and so on until the last pixel in the first row of the whole imaging area is read. The *col_out* signal 168 of the last imaging device in each row is connected back to the first device in the same row, as shown in Figure 8, and the row selector is advanced. The following rows are read in the same way until last row of the imaging device is reached and the *row_out* signal 172 is given a pulse enabling the first column in the next device in vertical direction. The *row_out* signal 172 of each device is connected to the *row_ena* signal 174 of next device in vertical direction. Each time the row selector is advanced to the next row, the previously selected row is reset. The whole area in the array of imaging devices is read using the same method. At the moment the last pixel in the whole area is read

and a pulse is present at the *col_out* signal 168 and *row_out* signal 172 of the last device, marked $U_{M,N}$, the sequence is started from the beginning provided that the *exp_mode* signal 176 is in a logic high state. The *exp_mode* signal 176 controls the running mode of the array. With the *exp_mode* signal 176 in low state, the system operates in single exposure mode reading the whole image area once. New *row_enable* 164 and *column_enable* 166 signals are required for starting another reading sequence. On the other hand, the same system can be used for continuously updating live video image by applying logic high level to the *exp_mode* signal 176. As long as the *exp_mode* signal 176 remains high, the reading sequence is started from the beginning once the last pixel in the whole area is reached.

In addition to the inputs shown in the Figure 8, clock input and the mode inputs for selecting the resolution are required, but for simplicity they are not shown in this example. Each of the imaging devices also includes the necessary circuitry for the programmable resolution described earlier. In case of using grouping of pixels for lowering the resolution, the read sequence is identical to the one described above except for the fact that several columns and rows are selected simultaneously and advanced in steps larger than one pixel according to the size of the pixel group.

The imaging system in Figure 8 can also be divided into two or more sections, each consisting of an array of imaging devices. In such arrangement each section is connected in the same way as described above for the whole imaging area. Such an arrangement produces more than one simultaneous output channels instead of just one.

An imaging device for radiation imaging system has been described. The imaging system consists of an array of several imaging devices. The number of devices in the array can be chosen according to the requirements of the target application, whether it is a small area system or a large area system. An imaging device as described herein has a capability to change the resolution of the device while the system is operating. The grouping of pixels into larger area super pixels is achieved by selecting several pixels at the same time. A pixel is selected when the row and column corresponding to the location of the pixel are selected simultaneously. With the method of operation explained herein, several columns and rows can be selected concurrently, thus selecting a group of pixels instead of just one. The

grouping of pixels has the advantage that the same system can be used for high-resolution still images as well as for lower resolution video applications. By grouping pixels directly in the imaging device, the amount of data is significantly reduced. Also, the speed and memory requirements for the image acquisition and processing system are reduced considerably.

The imaging device described herein can easily be applied for small and large area applications by connecting the end of row and end of column signals to the corresponding row enable and column enable signals on the next device in the array in read order.

CLAIMS

1. An imaging device for radiation imaging, said device comprising an array of detector cells for generating a charge in response to incident radiation, an array of cell circuits for accumulating charge generated, and control circuitry controlling output of signals from said cell circuits programmably to adjust the resolution of said imaging device.

2. An imaging device according to Claim 1, wherein said control circuitry is arranged to select a group of cell circuits and to produce an output signal representative of a sum of charge accumulated in all cell circuits in a said group.

3. An imaging device according to Claim 1 or Claim 2, wherein said control circuitry averages signals representative of charge accumulated in all cell circuits in said group.

4. An imaging device according to Claim 3, wherein said output signal is representative of the total charge for all of said cell circuits of said group divided by the number of cell circuits in said group.

5. An imaging device according to any one of Claims 2 to 4, wherein the number of cell circuits in a group is selectable from a set of possible numbers.

6. An imaging device according to any preceding Claim, wherein said output signal representative of charge accumulated is a current value.

7. An imaging device according to any preceding Claim, wherein said circuitry, for selecting a group of cell circuits, comprises a shift register arranged to select a plurality of columns or rows concurrently and to advance in steps of more than one row or column.

8. An imaging device according to Claim 7, wherein said control circuitry

additionally comprises logic arranged simultaneous to select a plurality of rows and columns and a step size larger than one.

9. An imaging device according to Claim 6, wherein said control circuitry is arranged to average currents from a group of cell circuits by connecting current outputs of each cell circuit into a common output node and dividing the resulting sum of currents by the number of pixels in said group using a current mirror.

10. An imaging device according to Claim 9, wherein said common output node holds a current of the selected cell circuit(s).

11. An imaging device according to Claim 2 or any Claim dependent thereon, wherein each cell circuit in said group, when operating in a group mode, produce a scaled output signal representative of charge accumulated in said cell circuit divided by a number of cell circuits in said group.

12. An imaging device according to Claim 11, operable in a plurality of group modes, where each group mode has associated with it a predetermined number of cell circuits, said cell circuits including an output transistor for each group mode, which output transistor produces said scaled output signal according to said number of cells in a selected group mode.

13. An imaging device according to Claim 12, wherein the said output signal from all cell circuits in said group is averaged by summing the signals together.

14. An imaging device according to any preceding Claim, comprising separate enabling signals for selecting columns and rows and output signals for indicating end of row or end of column.

15. An imaging device according to Claim 14, wherein said end of row and end of column output signals of one device are connected to corresponding enabling

signals of an adjacent device in first and second orthogonal directions, respectively, to form an array of imaging devices for larger area radiation imaging.

16. An imaging device according to any preceding Claim, wherein said array of detector cells and said array of cell circuits form an array of pixels.

17. An imaging system, comprising a plurality of imaging devices according to any preceding Claim connected as a two-dimensional array, whereby said imaging system provides selectable imaging resolutions for selected applications.

18. An imaging system according to Claim 17, wherein control circuitry is arranged to permit reading of cell circuits of one row of pixels across multiple imaging devices from the two-dimensional array of imaging devices, before proceeding to a subsequent row.

19. A method of operating an imaging device for radiation imaging, which device comprises of an array of detector cells for generating a charge in response to incident radiation, an array of cell circuits for accumulating charge generated, and control circuitry controlling output of signals from said cell circuits, said method comprising:

selecting a resolution of said imaging device;

adjusting addressing of said cell circuits to group outputs from said cell circuits according to a selected resolution.

20. An imaging device substantially as hereinbefore described with reference to the accompanying drawings.

21. An imaging system substantially as hereinbefore described with reference to the accompanying drawings.

22. A method of operating an imaging device substantially as hereinbefore described with reference to the accompanying drawings.

The Patent Office

18

Application No:	GB 9726768.6	**Examiner:**	Sue Willcox
Claims searched:	All	**Date of search:**	5 May 1998

Patents Act 1977
Search Report under Section 17

Databases searched:

UK Patent Office collections, including GB, EP, WO & US patent specifications, in:

UK Cl (Ed.P): H4F (FCCB, FCCX, FCCY, FEX, FGY, FJA)

Int Cl (Ed.6): H04N 1/04, 3/(14, 15), 5/(32, 33, 335)

Other: Online databases: WPI, Japio

Documents considered to be relevant:

Category	Identity of document and relevant passage		Relevant to claims
X, Y	WO 94/30004 A1	(Cambridge Imaging Ltd) see particularly page 2, lines 11 - 33; page 5, lines 4 - 11	X: 1, 2 Y: 3, 4
X	US 5581301	(Ninomiya) see particularly column 3, lines 54 - 63; column 4, lines 32 - 67	1, 2

X	Document indicating lack of novelty or inventive step	A	Document indicating technological background and/or state of the art.
Y	Document indicating lack of inventive step if combined with one or more other documents of same category.	P	Document published on or after the declared priority date but before the filing date of this invention.
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